

**BITLINE DIRECTION SHIELDING TO AVOID CROSS COUPLING BETWEEN  
ADJACENT CELLS FOR NAND FLASH MEMORY**

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**BACKGROUND OF THE INVENTION**

**Field of the Invention**

[0001] This invention relates generally to flash electrically erasable and programmable read only memory (EEPROMS), and more specifically to NAND flash memory with a high memory cell density.

**Related Art**

[0002] Most existing commercial flash EEPROM products operate each memory cell with two ranges of threshold voltages, one above and the other below a breakpoint level, thereby defining two programmed states. One bit of data is thus stored in each cell, a 0 when programmed into one state and a 1 when programmed into its other state. A chunk of a given number of bits of data is programmed at one time into an equal number of cells. The state of each cell is monitored during programming so that application of programming voltages stops when the threshold level of an individual cell is verified to have moved within the range that represents the value of the bit of data being stored in the cell.

[0003] In order to increase the amount of data stored in a flash EEPROM system having a certain number of storage cells, the individual cells are operated with more than two threshold level states. Preferably, two or more bits of data are stored in each cell by operating the individual cells with four or more programmable states. Three threshold breakpoint levels are necessary to define four different threshold states. Such a system is

described in U.S. Patent Nos. 5,043,940 and 5,172,338, which are hereby incorporated by this reference in their entirety. In multi-state operation, an available operating voltage range of the individual cells is divided into an increased number of states. The use of eight or more states, resulting in storing three or more bits of data per cell, is contemplated. The voltage range of each state necessarily becomes smaller as the number of states is increased. This leaves less margin within each state to accommodate any error that might occur during operation of the memory system.

[0004] One type of error is termed a "disturb," wherein electrons are unintentionally added to or taken away from a floating gate during operation of the memory. One source of a disturb is the presence of a leaky oxide dielectric positioned between the floating gate and another conductive gate of a cell. The charge level programmed onto a floating gate of a cell changes when such a leaky oxide is present, thus leading to the possibility that the state of the cell will be incorrectly read if the change in charge has been large enough. Since few to no errors can be tolerated in a mass digital data storage system, a sufficient margin for this error is provided by making the voltage range allocated to each state sufficient to include an expanded range of voltages that can occur as the result of such disturbs. This necessarily limits the number of states that can be included in a multi-state flash EEPROM system since the total available voltage range is limited.

[0005] Another type of error is termed the "Yupin effect." The Yupin effect occurs when the neighboring cell of a selected cell is programmed after the selected cell itself is programmed, and the charges of the neighboring cell influence the voltage of the selected cell. Such interference from the subsequently programmed neighbor cell distorts the voltages of the selected cell, possibly leading to an erroneous identification of its memory state during reading. Other program operations may also interfere with and influence the reading of a selected memory cell. The more compact a memory system becomes, the more influence a neighboring cell or operation has upon a selected cell.

## SUMMARY OF THE INVENTION

[0006] The present invention is an improved structure for high density NAND type flash memory that minimizes the effect of disturbs and Yupin effect errors. In one embodiment, adjacent floating gates in a string of memory cells are shielded from each other by conductive isolating members. This may reduce disturbs and Yupin effect errors in the bitline direction.

[0007] In another embodiment, the conductive isolating members are connected to control gates. Thus, conductive isolating members shield adjacent floating gates and also improve coupling between control gates and floating gates.

[0008] In another embodiment, a wordline that connects a row of control gates may shield adjacent floating gates in that row. The word line may be formed so that it extends into the trench isolation area that isolates adjacent strings of cells.

[0009] Another embodiment includes a process for fabricating isolating members between floating gates of an array of floating gates.

[0010] The present invention is better understood upon consideration of the detailed description below, in conjunction with the accompanying drawings of illustrative embodiments of the invention.

## BRIEF DESCRIPTION OF THE FIGURES

[0011] FIG. 1A is a plan view of the structure of memory array 100.

[0012] FIG. 1B is an electrical circuit diagram corresponding to the structure of FIG. 1.

[0013] FIG. 2 is a cross section of memory array 100.

[0014] FIG. 3 is a cross section of memory array 100.

[0015] FIG. 4 is a cross section of memory array 100.

[0016] FIG. 5 is a flow chart of a method of forming an embodiment of the present invention.

[0017] FIGS. 6A-6H are cross sections of memory array 100 at various stages during the fabrication process.

#### DETAILED DESCRIPTION OF THE INVENTION

[0018] The following is a detailed description of illustrative embodiments of the present invention. As these embodiments of the present invention are described with reference to the aforementioned drawings, various modifications or adaptations of the methods and or specific structures described may become apparent to those skilled in the art. All such modifications, adaptations, or variations that rely upon the teachings of the present invention, and through which these teachings have advanced the art, are considered to be within the scope of the present invention. Hence, these descriptions and drawings are not to be considered in a limiting sense, as it is understood that the present invention is in no way limited to the embodiments illustrated.

[0019] FIG. 1A illustrates a plan view of an embodiment of the NAND flash memory of the present invention. FIGS. 2-4 are cross sections taken through the structure shown in FIG. 1A. An electrical equivalent circuit of the memory array is given in FIG. 1B, wherein common elements within the structure of FIGS. 1A and 2-4 are identified by the same reference character.

[0020] Parallel wordlines 106 connect adjacent NAND strings of floating gates 102. The wordlines 106 are illustrated horizontally, and the strings are illustrated vertically in the figures. Wordlines 106 act as control gates for rows (as depicted) of floating gates. A NAND string generally includes a select gate followed by several floating gates and another select gate. The circuit diagram of FIG. 1B most clearly shows the vertical array of strings. In this case sixteen floating gates and thus sixteen wordlines are illustrated per string, however, the number of floating gates may be thirty-two or more, and is foreseen to increase in the future. Floating gates 102 are isolated from adjacent floating gates by isolation trenches 104. Isolation trenches 104 are also referred to as shallow trench isolation areas. The select gate line 105 on the source side ("SS") is continuous between trenches 104, as can be seen in section C-C of FIG. 4. It is not etched into individual floating gates. At the end of the wordline 106 above SS 105, each NAND string is electrically connected to SS 105 with a via, most easily seen in FIG. 1B and FIG. 3.

[0021] Metal bitlines 116 (only a portion of one is shown for the sake of clarity) connect to the N+ regions 114 within substrate 108 to sense amplifiers for reading the charge stored in the floating gates 102. The bitlines run parallel to the vertical array of strings. Thus, the bitlines have vertical axes, as do the strings in these illustrations. Thus, to read a particular floating gate a string is selected via the bitline and a wordline is also selected. The metal bitlines are generally, but not necessarily, formed in a conductive layer insulated from the wordlines. At the end of each string is another select gate coupled to the drain (“SD”). The drain and source can be interchanged in some configurations and more than 16 transistors can also be present in each string, thus also increasing the number of wordlines. Furthermore, any terms referring to the vertical or horizontal orientation are only used for ease of understanding and illustrative purposes, as the memory array can of course be depicted in different orientations.

[0022] Flanking each floating gate 102 are sidewalls 103. The sidewalls are protective or shielding elements that are located on the bitline sides of the floating gates 102. They may be thought of as being located on the bitline sides because they are located between floating gates in the same strings that are activated by the same bitlines 116, as will be discussed in more detail later with reference to FIG. 3. They may also be thought of as being in the bitline direction. Sidewalls 103 flank both a floating gate 102 and a wordline 106 located between a pair of sidewalls. The sidewalls 103 are also located between adjacent wordlines 106 because the wordlines are located directly above the rows of floating gates.

[0023] As seen in FIG. 2, there is a portion of gate oxide 112 between each floating gate 102 and the substrate 108. A dielectric material 110 separates the wordlines 106 from the floating gates 102 and the isolation trenches 104. Adjacent floating gates 102 are isolated from other floating gates in the same wordline, not only by isolating trenches 104, but also by wordlines 106. Wordlines 106 extend down between floating gates into isolation trenches 104, until, within, or past the level of gate oxide layer 112. This has three distinct benefits.

[0024] First, it reduces Yupin effects between adjacent cells in the wordline direction. Second, it improves the cell coupling ratio between the wordlines and the floating gates. The portion of the wordline that extends into the isolation trenches, to or past the depth of

the floating gates, increases the overlap of the surface areas and volumes of the wordlines and floating gates. This increased overlap results in better coupling when a charge is read or stored during program, read, or erase operations.

[0025] Third, the electrical field across the dielectric layer 110 between adjacent floating gates is reduced, therefore reducing any leakage current through the dielectric layer that may occur as a result of the electrical field. The lesser the electrical field, the lesser the leakage current between two adjacent floating gates. Additionally, the leakage current path is greatly increased by the extended wordlines 106. Any leakage current must travel down and around the extended portion of the wordlines and then back up or over to the adjacent floating gates. The charge level programmed onto a floating gate of a cell changes when such a leakage current is present. Therefore, by minimizing the leakage current, and thus any change in charge of the floating gates, an increased number of levels can be discerned more reliably. This leads to a higher capacity, more cost efficient, and more reliable data storage system.

[0026] As seen in FIG. 3, sidewalls 103 are located on the sides of floating gates 102 and wordlines 106. The sidewalls 103 preferably comprise primarily a conductive material such as polysilicon but may also comprise primarily another type of material such as an insulator or semiconductive material. Sidewalls 103 are electrically isolated from floating gates 102, as will be seen in more detail with reference to FIGS. 6A-H. The sidewalls as shown extend to the upper surface of wordlines 106 in the embodiment shown. However, the sidewalls may extend (in a direction away from substrate 108) to any level between the upper surface of floating gates 102 to the upper level of wordlines 106. Sidewalls 103 are preferably but not necessarily electrically connected or coupled to wordlines 106.

[0027] Although sidewalls 103 are shown as being substantially rectangular, the shape may vary and is secondary to the functionality of the sidewalls. Additionally when viewed with an electron microscope, structures rarely appear rectilinear. As discussed previously, memory arrays are subject to errors in read and write operations due to the adjacent charges and electrical fields. Sidewalls 103 serve to shield floating gates 102 from these adjacent fields. This reduces errors in reading and writing to the memory cells and allows for further miniaturization of the memory array.

[0028] In one embodiment where the sidewalls 103 comprise primarily (conductive) polysilicon and are electrically connected to the wordline 106 that they flank, the sidewalls also aid in the programming and reading of the floating gates. This is because, as most clearly seen in FIG. 3, the sidewalls 103, together with the wordlines 106 located between the sidewalls, envelope the floating gate. The surface area and coupling ratio are therefore greatly increased, and a charge may be more effectively written to or read from the enveloped floating gate. Thus, in addition to the aforementioned shielding benefit in read/write operations, the structure of the present invention also aids the read/write operations by increasing the coupling between the floating gates and wordlines (control gates).

[0029] FIG. 5 is a flowchart of some of the steps of making memory array 100 which should be referred to in tandem with FIGS 6A-6H. Note that only the main steps are described and illustrated.

[0030] The memory array 100 is fabricated in a substrate 108. Substrate 108 preferably comprises silicon but may also comprise any substrate material known to those in the art such as Gallium Arsenide etc. FIG. 5 describes the portion of making the memory array after the memory cells have already been created. The creation of the memory cells involves forming a first set of parallel trenches in the substrate, depositing an oxide layer within the first set of trenches, and forming a series of floating gates between the trenches of the first set of trenches. A second set of parallel trenches is formed in the oxide layer deposited within the first set of trenches. The formation also comprises forming a wordline above adjacent floating gates, the wordline extending into the second set of trenches thereby isolating one of the floating gates from a charge applied at an adjacent floating gate.

[0031] The creation of the memory cells is further described in U.S. Patent Application Serial No. 10/175764, entitled "deep Wordline Trench to Shield Cross Coupling between adjacent Cells for Scaled NAND," filed June 19, 2002, which is hereby incorporated by this reference in its entirety. U.S. Patent No. 5,867,429 entitled "High Density Non-Volatile Flash Memory Without Adverse Effects of Electric Field Coupling Between Adjacent Floating Gates" also contains information on the memory cells and is also hereby incorporated by this reference in its entirety. The specific sizes and materials of

the preferred embodiments described are only given for illustrative purposes hence the present invention should not be limited by these specific details given for ease of understanding.

[0032] In step 505, oxide 602 is grown upon the memory cells, as seen in FIG. 6A. Thermal oxide 602 is about 180 Angstroms thick +/- about 50 Angstroms and can also be other well known insulating layers such as TEOS, ONO, or SiN. Oxide 602 will not grow upon nitride 603 on the top of the memory cells. Next, a photoresist blanket 604 is deposited in step 510, as seen in FIG. 6B. Photoresist 604 is preferably an organic material such as Novoluk, but may be any type of photoresist known in the art. In step 515, the photoresist 604 is patterned and etched, leaving a portion of oxide 602 extending above/beyond the remaining photoresist 604, as seen in FIG. 6C. Photoresist 604 is precisely etched away to a level between the lower and upper surface of wordlines 106.

[0033] Next, in step 520, the oxide 602 is etched to form a contact for the "ears." It is etched down to, or below the level of photoresist 604 and as can be seen in FIG. 6D, there is a slight undercut 606 for the electrical contact of the ears with the wordlines 106. The ears are also interchangeably referred to as sidewalls throughout this application. Oxide 602 is preferably plasma etched but may also be wet etched or removed by any well known methods. In step 525 the photoresist 604 is removed as seen in FIG. 6E, preferably by reactive ion etching techniques.

[0034] In step 530 a conductive material 608 such as polysilicon is deposited upon the array seen in FIG. 6E. This is shown in FIG. 6F. Roughly 150 Angstroms of polysilicon is deposited.

[0035] In step 535, a protective layer 610 is deposited upon the conductive layer, as can be seen in FIG. 6G. Protective layer 610 may be made of a dielectric material such as a TEOS based oxide layer. Protective layer 610 serves to protect the underlying conductive material 608 during a subsequent etch through the protective layer 610 in step 545. In step 550 the protective layer 610 and conductive layer 608 are etched out of the peripheral area of memory array 100, i.e. the area generally not used for data storage. This is preferably done with a chemical plasma etch. In step 555, the photoresist is removed from the cell area. The cell area, unlike the peripheral area, is where the data is



stored. In step 560 the protective layer 610 and conductive layer 608 are etched out from between the cells. The area between each of the memory cells must be cleared in order to dope the source and drain (N+) regions 114, which although not formed until after step 560, have been shown in the figures for the sake of reference. The resultant structure shown in FIG. 6H illustrates memory array 100 after steps 540-560 have been performed.

[0036] While embodiments of the present invention have been shown and described, changes and modifications to these illustrative embodiments can be made without departing from the present invention in its broader aspects. Thus, it should be evident that there are other embodiments of this invention which, while not expressly described above, are within the scope of the present invention and therefore that the scope of the invention is not limited merely to the illustrative embodiments presented. Therefore, it will be understood that the appended claims set out the metes and bounds of the invention. However, as words are an imperfect way of describing the scope of the invention, it should also be understood that equivalent structures and methods while not within the express words of the claims are also within the true scope of the invention.